At page 12, kindly replace the third paragraph with the following amended paragraph:

FIGS. 11A and 11B depict the steps of forming a plurality of bit line stack patterns 134, bit line spacers, and a second bubble prevention layer. Specifically, a plurality of bit line stack patterns 134 are formed on the first filling insulating layer 126. The bit line stack patterns 134 function as the bit lines B/L shown in FIG. 5. Each bit line stack pattern 134 is formed by sequentially stacking a barrier metal layer 128, which is formed by sequentially forming Titanium (Ti) and Titanium Nitride (TiN) on the first filling insulating layer 126; a bit line conductive layer 130, which is formed by sequentially forming polysilicon and Tungsten Silicide (WSi) on the barrier metal layer 128; and a bit line capping layer 132, which may be formed of silicon oxide, or preferably silicon nitride Si_3N_4, and patterning the barrier metal layer 128, the bit line conductive layer 130 and the bit line capping layer 132. Holes 136 for exposing the first filling insulating layer 126 are formed between the bit line stack patterns 134.

A1

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

FIGS. 11A and 11B depict the steps of forming a plurality of bit line stack patterns 134, bit line spacers, and a second bubble prevention layer. Specifically, a plurality of bit line stack patterns 134 are formed on the first filling insulating layer 126. The bit line stack patterns 134 function as the bit lines B/L shown in FIG. 5. Each bit line stack pattern 134 is formed by sequentially stacking a barrier metal layer 128, which is formed by sequentially forming Titanium (Ti) and Titanium Nitride (TiN) on the first filling insulating layer 126; a bit line conductive layer 130, which is formed by sequentially forming polysilicon and Tungsten Silicide (WSi) on the barrier metal layer 128; and a bit line capping layer 132, which may be formed of silicon oxide, or preferably silicon nitride Si_3N_4, and patterning the barrier metal layer 128, the bit line conductive layer 130 and the bit line capping layer 132. Holes 136 for exposing the [semiconductor substrate 100] <u>first filling insulating layer 126</u> are formed between the bit line stack patterns 134.